Efficient Dynamic Bandwidth Re-allocation in Photonic Networks using SOI-based Microring Resonators

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Abstract: We propose a non-blocking, low-power, micro-ring resonator-based row-column switching matrix that can achieve dynamic bandwidth re-allocation by re-allocating bandwidth from under-utilized links to over-utilized links with less than 0.4% increase in power dissipation.

OCIS codes: (200.4650) Optical Interconnects; (250.6715) Switching

1. Introduction

The availability of small, low power, integratable optical switches is a key requirement to realize dense photonic integrated circuits (PICs) for High-Performance Computing (HPC) systems [1]. In this work, we propose an active row-column switch design for HPC systems that enables any-to-any non-blocking switching function. Silicon-on-insulator (SOI) based ring resonators are used to build 1×2 wavelength selective optical switches that are fast (~10ns), compact (~10μm diameter), power-efficient (~19μWatt) and can be fabricated using standard CMOS technology [2]. Two distinct advantages of using SOI based micro-ring resonators are: (1) They can be fabricated using existing CMOS technology, allowing for a low cost solution to dense PIC, and (2) They allow high confinement of light enabling micrometer scale devices, which results in low area and power overheads.

2. Proposed Architecture and Results

RAPID (**R**econfigurable **A**ll-**P**hotonic **I**nterconnected for **D**istributed parallel computers) is an opto-electronic network designed for HPC systems [3] as shown in Figure 1(a). Although static routing and wavelength assignment proposed in RAPID provides good performance for uniform and benign traffic patterns, considerable degradation in system performance is observed for adversial traffic due to uneven resource utilization. Dynamic bandwidth re-allocation (DBR) technique adapts to traffic patterns by re-allocating bandwidth from under-utilized links to over-utilized links. For RAPID architecture [3], we eliminate AWGs and replace them with row-column switches as shown in Figure 1(b). The row and column switches are themselves 2 × 2 switches. Due to the wavelength-selective nature of the rings, light at each input can be individually routed to any output. For an $n \times n$ switch matrix, we need n row and column switches. Analytical and simulation studies show that the proposed active implementation provides throughput and latency similar to the passive implementation while dramatically reducing the cost. There is a slight increase in power consumption (0.4% at most for the worst-case traffic) using the active switch matrix.

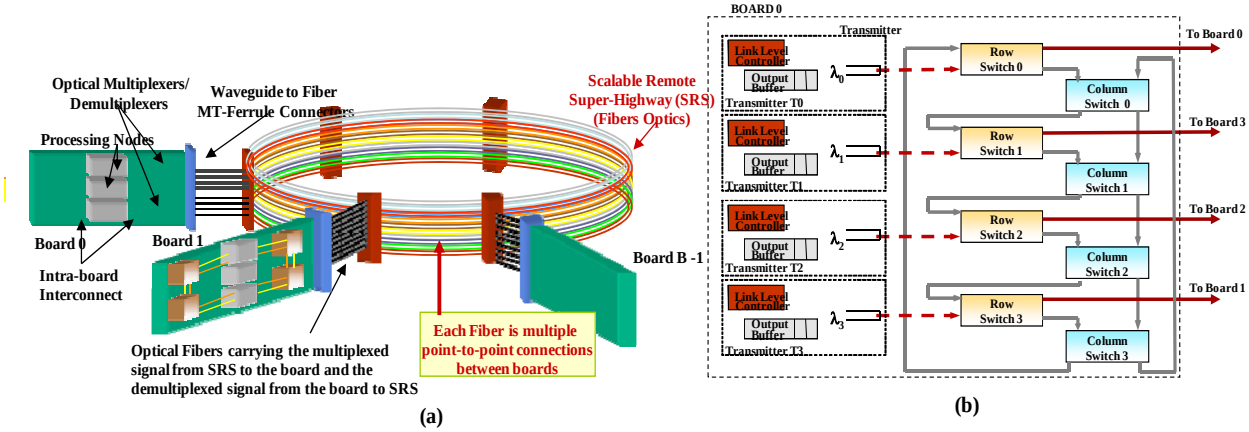

Figure 1: (a) RAPID architecture, and (b) Proposed row-column switching matrix for dynamic bandwidth re-allocation

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3. References

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