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Nanophotonic Interconnects and 3D-stacked Technology for Future Many-core Architectures

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Abstract: We explore silicon photonics and 3D stacked technology to implement a photonic network-on-chips. The proposed scheme provides 2.56 Tb/sec bandwidth with a much reduced power consumption and latency compared to any leading on-chip photonic networks.

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1. Introduction

Future chip multiprocessors (CMPs) will require high throughput and energy-efficient network-on-chips (NOCs). While metallic interconnects are facing fundamental physical limits as technology keeps scaling, optics has emerged as an alternative interconnect technology for NOCs [1]. Additionally, three-dimensional (3D) IC [2] design offers an exciting solution to further increase the integration density. Recent progress in depositing silicon waveguide in silicon dioxide makes it possible to integrate optical waveguide on different silicon layers [3].

2. Proposed Architecture

The proposed architecture is a multi-layer chip design for future CMPs as shown in Figure 1. The bottom layer, adjacent to the heat sink, contains 256 cores and local caches. One or more storage layers in the middle provide the bulk of on-chip storage. On top of the chip, several optical layers host the optical components and opto-electronic devices that are combined to provide photonic the infrastructure for on-chip and off-chip communications. The optical layers are built from known and established silicon photonic devices. On-chip optical power comes from off-chip laser source. Silicon Micro-ring resonators [4] are used as modulators, switches and multiplexers. The receivers are based on SiGe or Ge with limited power dissipation [5].

In our network topology, 256 cores are mapped as an 8x8 network with four-way concentration (four cores per node). In comparison with the global optical crossbar described in [1], the proposed topology consists of several partitioned optical crossbars mapped on different optical layers. Nodes on the same row or column form one partitioned crossbar. Intra-layer communications can be accomplished in a single hop, while inter-layer communications can be accomplished in two hops. An arbitration protocol is proposed to further reduce the latency. The proposed network can provide up to 2.56 Tb/s at much reduced power consumption and latency than any proposed on-chip photonic networks.

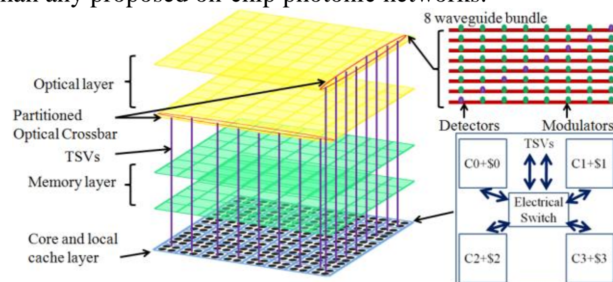

Figure 1: Proposed 3D architecture, TSV stands for Through-silicon vias.

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