Switchless Photonic Architecture for Parallel Computers

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Abstract: The design and analysis of a switchless, scalable, all-photonic architecture for high-performance parallel and distributed computers using passive optical interconnect technology is discussed.

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1. Introduction

One of the fundamental problems in parallel computers is the ever-increasing speed of the processors themselves and the growing performance gap between processor and the interconnect technologies [1]. Moreover, Moore's Law states that microprocessor speed doubles every 18 months or so that will require corresponding increase in bandwidth requirements. As data communication performance increases far more slowly, bandwidth (both memory and communication) will be a major and critical resource in the future. It is necessary that these short-range communication networks must be built on scalable architectures for systems to operate at maximum speed.

2. Architecture Overview

One technology that has the potential for providing higher bandwidths, lower crosstalk, zero EMI, and lower latencies at lower power requirements than current electronics-based interconnect is the optical interconnect technology [2]. This paper proposes an integrated solution to solve the remote memory access latency in parallel computers and still be able to scale the network significantly using optical technology for both board-to-board and backplane communications using passive technology. As a solution, we proposed an optical interconnect called **RAPID** (Reconfigurable All-Photonic Interconnect for Distributed and parallel computers)[3] as shown in Figure 1. RAPID reduces remote memory access latency by (1) increasing the connectivity, maximizing the channel availability and providing scalable bandwidth using a combination of WDM, TDM and SDM techniques; (2) using a decentralized wavelength allocation scheme along with efficient re-use of the available wavelengths and (3) using a switchless topology that is based on passive optical interconnect technology that reduces the cost and improves performance significantly. We have extended RAPID architecture to include clusters, proposed the implementation of RAPID at the board, inter-board and inter-cluster levels. We have evaluated the performance of RAPID using RSIM and found that RAPID outperforms mesh electrical network by 40%. RAPID fully utilizes the benefits of WDM along with SDM and TDM to produce a highly scalable, high bandwidth network with low overall latency that could be very cost effective to produce.

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3. References

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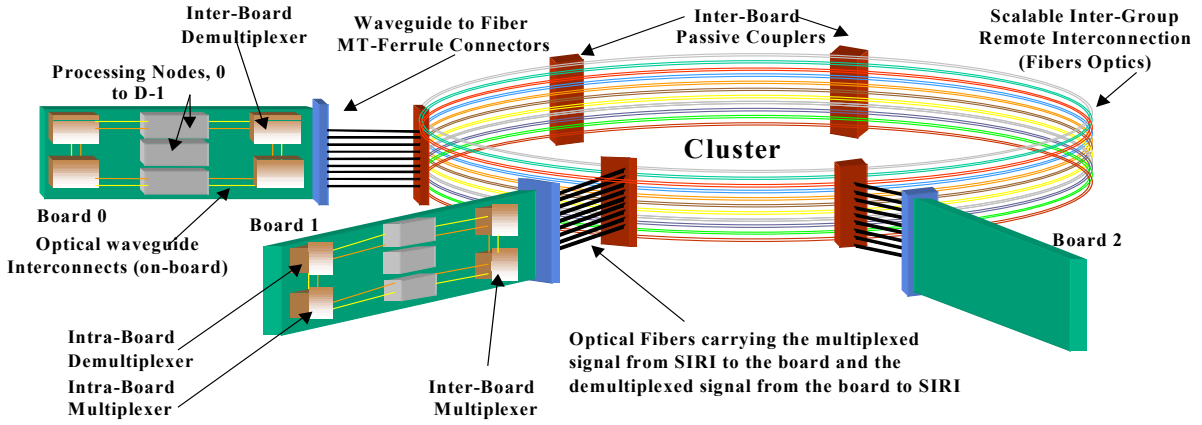

Figure 1: RAPID architecture