J. Parallel Distrib. Comput. 71 (2011) 623–624

Contents lists available at ScienceDirect

J. Parallel Distrib. Comput.

journal homepage: www.elsevier.com/locate/jpdc

Editorial

Introduction to the special issue on Networks-on-Chip (NoC) of the Journal of Parallel and Distributed Computing (JPDC)

It is with great pleasure that we introduce the special issue on Networks-on-Chip (NoC) to the readers of the Journal of Parallel and Distributed Computing (JPDC). This special issue consists of eight peer-reviewed papers that cover a wide spectrum of topics in NoC design.

Large multicore-based and multiprocessor-based systems-on-chip (MPSoC) architectures will easily consist of billions of transistors according to projected technology roadmaps. The complexity in integrating hundreds of cores running simultaneously on a single chip calls for a serious need to revisit the on-chip communication infrastructure. The new on-chip communication paradigm that can effectively address and overcome the design issues is called the Networks-on-Chip (NoC) paradigm. This special issue focuses on how to meet some of the design challenges posed by current and future NoCs in scalable multicore architectures.

The NoC paradigm provides the scalable infrastructure with which we can integrate a large number of computational logic and storage blocks on a single chip. While traditional bus-based networks and point-to-point networks can provide communication bandwidth, they suffer from increased power dissipation and contention or latency issues. Therefore, the NoC paradigm has evolved from the desire to have an infrastructure that can be easily scaled and modularly expanded. With modular and regular communication paths, NoCs enable path diversity, reusability and predictability, which, when combined, reduce network congestion, alleviate power dissipation, and provide enhanced reliability.

Mobile handsets, wireless chipsets, portable multimedia and cell phones are just a few applications which make use of MPSoC. In these energy-constrained environments, performance, power consumption and delivery, reliability, fault tolerance, error recovery and hardware costs of the underlying communication fabric (NoC) are posing serious design challenges. Moreover, implementation, testing, yield, modeling and quality of service (QoS) are also related to the practical realization of these systems. With technology scaling, concerns about metallic interconnects for NoC and their scalability into the subnanometer regime are also being debated.

With the goal of exploring how the research community is aggressively meeting these challenges, this special issue brings together outstanding experts from both academia and industry who have made significant contributions to the area of NoC design. The first paper in the special section is "RAFT: A Router Architecture with Frequency Tuning for On-chip Networks", by Asit K. Mishra, Aditya Yanamandra, Reetuparna Das, Soumya Eachempati, Ravi Iyer, N. Vijaykrishnan, and Chita R. Das. In this paper, the authors propose to minimize the power dissipation in on-chip networks by tuning the frequency of the router port in response to the traffic load. The authors propose several techniques which target congestion and power management in NoC routers using DVFS (dynamic voltage and frequency scaling), and optimize the imbalance in the router pipeline via time stealing. This work targets router microarchitecture design where frequency tuning relates to improving the overall reduction in power consumption while improving performance.

The second paper is "Time-Division-Multiplexed Arbitration in Silicon Nanophotonic Networks-On-Chip for High-Performance Chip Multiprocessors", by Gilbert Hendry, Eric Robinson, Vitaliy Gleyzer, Johnnie Chan, Luca P. Carloni, Nadya Bliss and Keren Bergman. In this paper, the authors propose to utilize the emerging technology of silicon nanophotonics as an interconnect technology for on-chip communication. Silicon nanophotonics is a disruptive technology solution which offers energy-efficient end-to-end transmission that is largely independent of the datarate and distance. In this paper, the authors improve the arbitration aspect of their circuit-switched set-up path in their all-optical broadband network. Time-division multiplexed (TDM) arbitration proposed by the authors improves the interconnect bandwidth between the communicating pairs and provides better network resource utilization while providing round-robin fairness.

The next three papers included in the special section discuss the issues of testing, reliability, and yield characterization. The first of the three papers is "Characterizing the Impact of Process Variation on 45 nm NoC-Based CMPs", by Carles Hernández, Antoni Roca, Federico Silla, Jose Flich and José Duato. In this paper, the authors target the important problem of process variation associated with integration of large-scale chip multiprocessors (CMPs). As variability causes the delay of links and routers to mismatch from the initial design, the authors analyze the impact of variability on an 8×8 mesh architecture using 45 nm technology. The paper also analyzes the communication bottlenecks on a GALS framework due to slower components, which in turn increase congestion and reduce performance. The authors clearly highlight the need to account for variability in the design, and show substantial performance benefits when this is accounted for in a CMP environment. The second of the three papers is "Improving the Yield of NoC-based Systems through Fault Diagnosis and Adaptive Routing", by Caroline Concatto, Fernanda G Kastensmidt, Fernanda Gusmão de Lima Kastensmidt, João Almeida, Guilherme Fachini, Marcos Hervé, Erika Cota and Marcelo Lubaszewski. In this paper, the authors propose an effective and low-cost method to increase the yield of NoCs by diagnosing and detecting faults using built-in self-test (BIST) structures and activating alternate paths for faulty links. The authors propose and develop their interconnect

0743-7315/$ – see front matter
doi:10.1016/j.jpdc.2011.01.010

fault model which consists of both stuck-at faults and pairwise shorts within a link or between any two links for a 3×3 torus network. Their result yield a higher reliability with minimum performance and area penalty. The third of the three papers is "A New Test Scheduling Algorithm Based on Networks-on-Chip as Test Access Mechanisms", by Alexandre Amory, Cristiano Lazzari, Marcelo Lubaszewski and Fernando Moraes. The authors propose a new test environment in which the designer can quickly evaluate the wiring and testing time for various test architectures. The paper also discusses a new testing schedule for NoC test access mechanisms (TAMs) which does not require any NoC timing information while having the capability to model different NoC topologies.

The last three papers of the special section tackle the issues of QoS and modeling intrachip communication in NoC architectures, which are becoming an important issue in NoC architectures. The first of the three papers is "Static Timing Analysis for Modeling QoS in Networks on Chip", by Evgeni Krimer, Isaac Keslassy, Avinoam Kolodny, Isask'har Walter and Mattan Erez. In this paper, the authors propose a methodology that involves a static packet-level timing analysis which can quickly gauge the performance of virtual channel wormhole NoC without simulation. The proposed network models any topology, link capacity and buffer size while providing per-flow delay analysis that is an order of magnitude faster than simulation, paving the way for faster analysis of NoC architectures. The second of the three papers is "CoQoS: Coordinating QoS-Aware Shared Resources in NoC-Based SoCs", by Bin Li, Li Zhao, Ravi Iyer, Li-Shiuan Peh, Michael Leddige, Michael Espig, Seung Eun Lee and Donald Newell. The authors propose a class-for-service-based QoS architecture (CoQoS) which jointly manages three performance-critical resources, namely cache, NoC and memory in an NoC-based SoC platform. The authors evaluate and study the problem of efficient resource allocation in an SoC environment and provide a low-cost solution. The last of the three is "CAFES: A Framework for Intrachip Application Modeling and Communication Architecture Design", by César A. Marcon, Ney Laert Vilar Calazans, Edson I. Moreno, Fernando G. Moraes, Fabiano P. Hessel and Altamiro A. Susin. The authors propose CAFES, an open-source framework that supports several tasks related to high-level modeling and design of applications employing complex intrachip communication infrastructures with several case studies, underlying a modeling framework for NoCs.

We sincerely hope that you will enjoy this special issue. We believe that NoC is an important research topic and that it will continue to grow in significance for a wide range of applications in the future. We hope that this issue will remain an important reference for future publications and help in continuous advancement of the field. We thank all the authors for their excellent contributions to this issue. We also gratefully acknowledge all the reviewers for their efforts in shaping this special issue. Finally, we thank the Editors of JPDC (Prof. Allan Gottlieb, Prof. Kai Hwang and Prof. Sartaj Sahni) for supporting and encouraging this topic, and Ms. Amy Mutale for providing excellent support with the submission and peer-review process. We sincerely hope that you enjoy and appreciate this special issue.

Guest editors
Ahmed Louri
Department of Electrical and Computer Engineering, University of Arizona Tucson, AZ 85721, United States
E-mail address: louri@ece.arizona.edu.

Avinash Karanth Kodi*
School of Electrical Engineering and Computer Science, Ohio University Athens, OH 45701, United States
E-mail address: kodi@ohio.edu.

Available online 26 January 2011

* Corresponding editor.