Parallel Optical Interconnection Network for SMPs

Ahmed Louri and Avinash Karanth Kodi
Department of Electrical and Computer Engineering, University of Arizona, Tucson, AZ-85721
Tel: (520)-621-2318; Fax: (520)-621-8076; e-mail: louri@ece.arizona.edu

Abstract: We propose a scalable address sub-network called Symmetric Multiprocessor Network (SYMNET) to solve the address bandwidth limitation in SMPs. Our simulation studies have shown 5-66% improvement in execution time and 5-78% improvement in average latency for SYMNET as compared to the electrical bus-based SMPs for various Splash-2 benchmarks.

OCIS codes: (200.4650) Optical Interconnects, (200.4960) Parallel Processing.

1. Introduction

Symmetric Multiprocessors (SMPs) use fast snooping protocols to maintain cache coherence and is facilitated by the time-multiplexed shared-bus. Contention to acquire the bus in addition to faster processing capabilities of current processors (2-3GHz) degrades the performance of the shared-bus. This limits the number of processors that can be connected to the bus, thereby affecting scalability of SMPs. Therefore the snoop or address bandwidth required for broadcasting the address requests is the major limitation of SMPs [1].

2. Architecture Overview

One technology that can provide high communication bandwidth, low latency and scalability is optical interconnection technology. The proposed optical symmetric multiprocessor network called SYMNET consisting of four processors/memory modules interconnected is shown in figure 1. The address sub-network is constructed using dual array of Y-couplers, which is a two-way address transmission (see the inset in figure 1). The up-stream array of Y-couplers is used for combining the address requests from the processors. After reaching higher levels, this address request is re-routed through the downstream array of Y-splitters which enable broadcasting of the address requests to all the processors and memories. Time division multiple access (TDMA) protocol is used as a control mechanism to achieve mutual exclusive access to the shared channel. A possible optical implementation of SYMNET [2] using parallel optical transceivers, polymer waveguides and arrays of y-couplers/splitters is shown in figure 2. SYMNET not only has the ability to pipeline address requests, but also multiple address requests from different processors can propagate through the address sub-network simultaneously [2]. Cache coherence cannot be maintained by using standard snooping-protocols. Therefore, it is modified to take into account the simultaneous insertions of multiple address requests into the sub-network. Coherence in SYMNET, called COSYM is modified from the popular MOESI (Modified, Owned, Exclusive, Shared, Invalid) protocol. We used Limes (Linux Memory Simulator), and evaluated COSYM with the electrical bus-based MOESI coherence protocol with a subset of Splash-2 benchmarks. Our simulation studies have shown a 5-66% improvement in execution time and 5-78% improvement in average latency for COSYM protocol as compared to MOESI protocol for various applications [2].

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3. References

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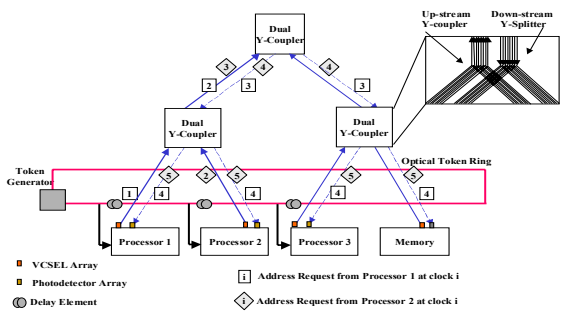

Fig 1: An overview of SYMNET architecture consisting of processors and memory modules.

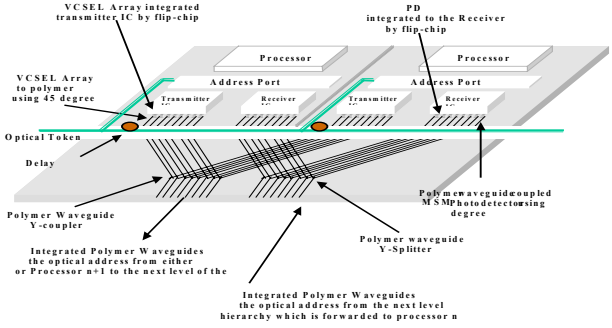

Fig 2: A possible implementation of SYMNET using parallel optical interconnections.